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## (54) IMPROVEMENTS IN THE MANUFACTURE OF SEMICONDUCTOR DIODES

(71) We, HITACHI LIMITED of 1-5-1 Marunouchi, Chiyoda-ku, Tokyo, Japan, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to a semiconductor diode having at least one p-n junction therein and a method for making the diode. More particularly the invention relates to a semiconductor diode, an electrical characteristic of which, is controlled by varying an electrical characteristic of the p-n junction.

As is well known, p-n junctions are utilized in a lot of semiconductor devices, such as diodes and transistors, in order to achieve their desired electrical characteristics.

More recently, electrical characteristics of the p-n junction, such as the capacitance characteristic and the break-down characteristic have been utilized in semiconductor diodes of the variable capacitance and zener diode types.

It is well known that these semiconductor diodes, that is, the variable capacitance diode and the zener diode, in other words those semiconductor diodes which utilize the capacitance characteristic and the break-down characteristic of a p-n junction, are much influenced by an impurity concentration in the semiconductor body.

A conventional semiconductor diode utilizing the capacitance characteristic or the break-down characteristic of a p-n junction comprises a semiconductor body; a first semi- impurity concentration is higher than that of the body, and whose conductivity type is the same as that of the body; a second semiconductor region disposed in the semiconductor body and over the first semiconductor region, whose impurity concentration is higher than that of the first semiconductor region, and whose conductivity type is opposite to that of the first semiconductor region, thereby forming a p-n junction at least between the first semiconductor region and the second semiconductor region; and electrodes formed on the second region and on the semiconductor body.

In this known semiconductor diode, the first semiconductor region is a region having an impurity concentration distribution which prescribes a variation of capacitance in the variable capacitance diode, and a reverse break-down voltage in the zener diode. Therefore, the semiconductor diode should have a strictly controlled impurity concentration distribution for obtaining a wide variable range of capacitance and a high break-down voltage.

According to the present invention there is provided a semiconductor dode utilizing a capacitance characteristic and a break-down characteristic of a p-n junction including: a semiconductor body having a mesa shaped portion; a semiconductor layer disposed in the semiconductor body at the surface of the mesa shaped portion, whose conductivity type is opposite to that of the semiconductor body, thereby forming a p-n junction between the semiconductor layer and the semiconductor body; at least one semiconductor region disposed in the semiconductor body immediately below the semiconductor layer, having a conductivity type the same as the semiconductor body, thereby forming a p-n junction between the semiconductor region and the semiconductor layer being encircled by the p-n junction between the semiconductor layer and the semiconductor body; and electrodes formed on the semiconductor layer and the semiconductor body, respectively.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:—

Figure 1 is a sectional view of a conventional planar type variable capacitance diode;

Figure 2 is a sectional view of a conventional mesa type variable capacitance diode;

Figure 3 is a sectional view of one preferred

embodiment of a diode made in accordance with the present invention;

Figures 4*a* to 4*e* are sectional views of the diode which assist in explaining the method of producing the diode shown in Figure 3;

Figure 5*a* to 5*f* are sectional views of a variable capacitance diode for explaining another method of manufacturing such a semiconductor diode; and

Figure 6 is a graph showing capacitance plotted to a base of applied voltages for the semiconductor diode shown in Figure 5.

Referring now to Figure 1 which shows a sectional view of a conventional semiconductor diode, utilizing the capacitance characteristics and the break-down characterisic of a p-n junction, formed by a diffusion method. This semiconductor diode comprises a semiconductor body 1, a first semiconductor region 2 formed selectively by diffusion in the semiconductor body 1, whose conductivity type is the same as that of the semiconductor body 1, a second semiconductor region 3 formed by diffusion in the semiconductor body 1 and over the first semiconductor region 2, whose conductivity type is opposite to that of the semiconductor body 1 and the first semiconductor region 2, thereby forming p-n junction between the first semiconductor region 1 and the second semiconductor region 2, and between the semiconductor body 1 and the second semiconductor region 3, and between electrodes 4 and 5 which are located respectively on the second semiconductor region 3 and on the semiconductor body 1. An insulating layer 6 is provided on the semiconductor body 1 for insulating the electrode 4 from the semiconductor body 1.

In this conventional semiconductor diode, since the first and second semiconductor regions are formed by a diffusion method it is very difficult to control accurately the impurity concentration. Therefore, the yield rate of the diode becomes low, and the break-down voltage is limited. Practically, the break-down voltage of the semiconductor diode is less than 25 V.

To avoid such disadvantages, it is proposed that the first semiconductor region 2 in Figure 1 is formed by an ion implantation method which provides a controlled impurity concentration distribution in the semiconductor body 1.

When the first semiconductor region is formed by the ion implantation method, the depth of the first semiconductor region is limited to about 0.25μ, since the energy of ions, for forming impurity regions is usually 100 KeV—200 KeV. Therefore, the depth of p-n junction is limited to less than that of the first semiconductor region, that is, less than 0.25μ. Though the depth of the first semiconductor region depends on the ion energy, usually the ion energy is limited to 100 KeV—200 KeV as described above, since the higher the ion energy, the more damage is done to the surface of the semiconductor body.

Since the p-n junction is formed in a thin layer of the semiconductor body, the radius of curvature of the p-n junction becomes very small, therefore the electrical field is concentrated in the curved portion of the p-n junction, and hence the break-down voltage of the semiconductor diode becomes lower.

In order to avoid this disadvantage, that is, the lowering of the break-down voltage of the shallow planar junction, a mesa shaped semiconductor diode has been proposed.

Figure 2 shows a sectional view of a mesa shaped semiconductor diode which comprises a semiconductor body 10 having a mesa shaped portion, a first semiconductor layer 11 disposed in the mesa shaped portion of the body 10, whose conductivity type is the same as that of the semiconductor body 10 and whose impurity concentration is higher than that of the semiconductor body 10, a second semiconductor layer 12 disposed in the semiconductor body 10 and over the first semiconductor layer 11, whose conductivity type is opposite to that of the first semiconductor layer 11 and whose impurity concentration is higher than that of the first semiconductor layer 11, thereby forming a p-n junction 13 between the first and second semiconductor layers 11 and 12, and between electrodes 15 and 16 which are located respectively on the second semiconductor layer 12 and on the semiconductor body 10.

This p-n junction 13 extends to the side of the mesa shaped portion and is exposed to the atmosphere at the sides. Therefore, a passivation film 14, such as a silicon dioxide ($SiO_2$) layer is disposed on the side surface portion of the semiconductor body 10 as shown in Figure 2.

Since the passivation film 14 usually includes metal ions, such as Sodium (Na) ions, when an $n^-$ conductivity type semiconductor material is utilized as the semiconductor body 1, that is, the first semiconductor layer 11 is $n$ type, and the second semiconductor layer 12 is $p^+$ type, the conductivity type of the surface portion 17 of the first semiconductor layer 11 adjacent to the side of the mesa shaped portion is changed to $n^+$ conductivity type. Therefore the $p^+$—$n$ junction 13 is changed to $p^+$—$n^+$ junction at the surface portion 17, and the break-down voltage of the semiconductor diode becomes low. And when a $p^-$ conductivity type semiconductor material is utilized as the semiconductor body 1, that is, the first semiconductor layer 11 is $p$ type, and the second semiconductor layer 12 is $n^+$ type, the conductivity type at the surface portion of the first semiconductor layer 11 and the semiconductor body 10 next to the passivation film 14 is changed to an $n$ conductivity type. Therefore, between the surface portion,

and the first semiconductor layer 11 and the semiconductor body 10, a p-n junction is formed. This means that the original p-n junction 13 extends along the surface portion of the first semiconductor layer 11 and the semiconductor body 10. Thus, there is a large leakage current, and hence it is very difficut to obtain the desired characteristic of the semiconductor diode.

These above mentioned disadvantages are overcome by the semiconductor diode shown in Figure 3. The semiconductor diode includes a semiconductor body 20 having a mesa shaped portion, a semiconductor layer 21 disposed at the surface portion of the mesa shaped portion of the semiconductor body 20, whose conductivity type is opposite to that of the semiconductor body 20, and a semiconductor region 22 disposed in the semiconductor body 20 immediately below the semiconductor layer 21, the conductivity type of the region being opposite to that of the semiconductor layer 21 and the impurity concentration of which is higher than that of the semiconductor body 20. A p-n junction 23 is thus formed between the semiconductor layer 21 and the semiconductor region 22 and is encircled by a p-n junction 24 which is formed between the semiconductor layer 21 and the semiconductor body 20. Electrodes 25 and 26 are located on the semiconductor layer 21 and the semiconductor body 20, respectively.

One preferred method of manufacturing the semiconductor diode shown in Figure 3 is now described wtih reference to Figures 4a to 4e.

Into the surface portion of an *n*-type semiconductor body 20 having a resistivity of 1 ohm-cm, that is, an impurity concentration of about $5\times10^{15}$ atoms/cm$^3$, an impurity of boron is diffused by heating the body 20 at about 300°C for 20 minutes, thereby forming a semiconductor layer 21 whose depth is about 4.15$\mu$ as shown in Figure 4a. This body 20 is mesa etched for 1 minute by an etching solution of HF and $HNO_3$ whose volume ratio is 1:40 to produce the shape shown in Figure 4b. A passivation film 27, consisting of an $SiO_2$ film whose thickness is about 3000Å and a phospho-silicate glass layer on the $SiO_2$ film, whose thickness is about 4000 Å, is formed on the surface of the semiconductor body 20 by a chemical vapour deposition method. A through hole 28 is formed in the desired central portion of the passivation film 27 by an etching technique as shown in Figure 4c. Next, a phosphorous ion radiation 29 whose energy is 200 KeV is directed onto the semiconductor body 20 in the region of the through hole 28, whereby a semiconductor region 22 is formed in the semiconductor body 20 immediately below the semiconductor layer 21, and also a p-n junction 23 is formed between the semiconductor layer 21 and the semiconductor region 22, so as to be encircled by a p-n junction 24 between the semiconductor layer 21 and the semiconductor body 20 as shown in Figure 4d. After the ion implantation, the semiconductor body 20 is heated to about 900°C for 10 minutes, and the electrodes 25 and 26 are formed on the semiconductor layer 21 and on the semiconductor body 20, respectively (Figure 4e).

The break-down voltage of the semiconductor diode is about 35 V. This value of the break-down voltage is higher than those of the conventional semiconductor dodes.

In the above described embodiment, although only one semiconductor region 22 is disposed in the semiconductor body 20, two or more such semiconductor regions can be disposed in the semiconductor body to obtain a semiconductor diode having a desired voltage dependency on the capacitance of the p-n junctions between the regions and the layer.

Figures 5a to 5f illustrate a preferred method for producing a semiconductor diode in which two semiconductor regions are disposed in a semiconductor body.

An impurity of boron is diffused into a surface portion of a semiconductor body 30 having a resistivity of 1 ohm-cm, at a temperature of about 900°C, for 20 minutes, thereby forming a boron diffused layer semiconductor layer 31 having a thickness of about 0.15$\mu$ as shown in Figure 5a. This semiconductor body 30 is etched for one minute, in a mesa shape as shown by Figure 5b by an etching solution of HF and $HNO_3$ whose volume ratio is 1:40. A passivation film 32 is formed on the surface of the semiconductor body 30 by a chemical vapour deposition method, and a first through hole 33 is formed in the passivation film 32 at the desired location as shown in Figure 5c. Next, phosphorous ion radiation 34 whose energy is about 50 KeV is directed onto the semiconductor body through the through hole 33 thereby forming a first semiconductor region 35 in the semiconductor body 30 immediately below the semiconductor layer 31, so that a p-n junction 36 between the semiconductor layer 31 and the first semiconductor region 35 is encircled by a p-n junction 37 between the semiconductor layer 31 and the semiconductor body 30 as shown in Figure 5d. Next, a $SiO_2$ layer 38 is formed on the exposed surface of the semiconductor body 30 an on the passivation film 32, and a second through hole 39 is formed in a different area from that at which the first through hole 33 was formed, as shown in Figure 5e. Next, phosphorous ion radiation 40 whose energy is about 300 KeV is directed onto the semiconductor body in the region of the through hole 39, thereby forming a second semiconductor region 41 in the semiconductor body 30 immediately below the semiconductor layer 31 different from the first semiconductor region 35, so that a p-n

junction 42 between the semiconductor layer 31 and the second semiconductor region 41 is encircled by a p-n junction 37 between the semiconductor layer 31 and the semiconductor body 30 as shown in Figure 5*e*. After the ion implantation, the semiconductor body is heated to a temperature of about 900°C for 10 minutes, and then a part of the $SiO_2$ layer 38 which corresponds to the first semiconductor region 35 is etched, thereby forming a through hole. After that, electrodes 43 and 44 are formed on the exposed surface of the semiconductor layer 31 and the semiconductor body 30 as shown in Figure 5*f*.

Figure 6 shows the relationship between capacitances of the first semiconductor region 35 and the voltages applied to the electrodes, between capacitances of the second semiconductor region 41 and the voltages applied to the electrodes, and between capacitances of the first and second semiconductor regions and the voltages applied to the electrodes.

In Figure 6, the ordinate denotes capacitance in picofarads, the abscissa denotes applied voltages, and curves *a*, *b* and *c* show the relationship between capacitance and voltage at the first semiconductor region, at the second semiconductor region, and at the first and second semiconductor regions combined, respectively.

As can be seen from curves *a*, *b* and *c* shown in Figure 6, the voltage dependency on capacitance at the first and second semiconductor regions combined, that is the semiconductor diode shown in Figure 5 is more linear than those at the first semiconductor region alone, and also at the second semiconductor region alone. Accordingly, a semiconductor diode utilizing the capacitance characteristics and the break-down characteristic of a p-n junction having high break-down voltages is obtained. Moreover, since mesa shaped semiconductor devices can be tested before the formation of the semiconductor region or regions, the yield rate of the semiconductor dode becomes high.

It will be appreciated that as in the case of the prior art construction referred to with reference to Fig. 2, the semiconductor body in one form can be of $\pi^-$-type, the semiconductor region can be of *n*-type, whilst the semiconductor layer can be of $p^+$-type.

WHAT WE CLAIM IS:—

1. A semiconductor diode utilizing a capacitance characteristic and a break-down characteristic of a p-n junction including: a semiconductor body having a mesa shaped portion; a semiconductor layer disposed in the semiconductor body at the surface of the mesa shaped portion, whose conductivity type is opposite to that of the semiconductor body, thereby forming a p-n junction between the semiconductor layer and the semiconductor body; at least one semiconductor region disposed in the semiconductor body immediately below the semiconductor layer, having the same conductivity type as the semiconductor body, thereby forming a p-n junction between the semiconductor region and the semiconductor layer; said p-n junction between the semiconductor region and the semiconductor layer being encircled by the p-n junction between the semiconductor layer and the semiconductor body; and electrodes formed on the semiconductor layer and the semiconductor body, respectively.

2. A semiconductor diode according to claim 1, wherein said semiconductor region is formed by an ion implantation.

3. A semiconductor diode according to clain 1 or 2, wherein said semiconductor body is of $\pi^-$-type, said semiconductor region is of *n*-type, and said semiconductor layer is of $p^+$-type.

4. A semiconductor diode according to any one of the preceding claims, further including a passivation film disposed on the exposed surface of the semiconductor body.

5. A semiconductor diode according to claim 4, wherein said passivation film consists of a $SiO_2$ film and a phospho-silicate glass film.

6. A semiconductor diode according to claim 1, wherein a second semiconductor region is disposed in the semiconductor body immediately below another part of the semiconductor layer, whose conductivity type is the same as that of the semiconductor body, thereby forming a second p-n junction between the semiconductor layer and the second semiconductor region; said first and second p-n junctions between the semiconductor layer and the first and second semiconductor regions, respectively being encircled by the p-n junction between the semiconductor layer and the semiconductor body.

7. A semiconductor diode according to claim 6, wherein said first and second semiconductor regions are formed by an ion implantation.

8. A semiconductor diode according to claim 6 or 7, further including a passivation film disposed on the exposed surface of the semiconductor body.

9. A method of manufacturing a semiconductor diode utilizing a capacitance characteristic and a break-down characteristic of a p-n junction including the steps of: preparing a semiconductor body having a mesa shaped portion; diffusing impurities, which change the conductivity type of the semiconductor body, into the surface portion of the mesa shaped portion of the semiconductor body, thereby forming a semiconductor layer whose conductivity type is opposite to that of the semiconductor body, and forming a p-n junction between the semiconductor body and the semiconductor layer; implanting ions

which show the same conductivity type as that of the semiconductor body into the semiconductor body immediately below the semiconductor layer, so as to form an ion implantation region whose boundary to said semiconductor layer is encircled by the p-n junction formed between the semiconductor layer and said body; and forming electrodes on the semiconductor layer and on the semiconductor body, respectively.

10. The method according to claim 9, wherein the semiconductor body is etched to form the mesa shape by an etching solution of hydrofluoric acid and nitric acid.

11. The method according to claim 9 or 10, wherein the step of implanting ions is carried out by directing phosphorus ion radiation into the semiconductor body.

12. A semiconductor dode constructed and arranged to operate substantially as herein described with reference to and as illustrated in Figure 3, or Figure 4*e*, or Figure 5*f* of the accompanying drawings.

13. The method of manufacturing a semiconductor diode substantially as herein described with reference to and as illustrated in Figures 4*a* to 4*e* or Figures 5*a* to 5*f* of the accompanying drawings.

14. A variable capacitance diode or zener diode manufactured in accordance with the method claimed in any one of claims 9 to 11.

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Sheet 1

FIG. 1

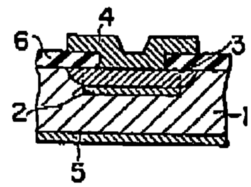



FIG. 2

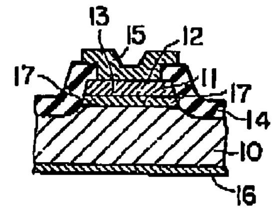



FIG. 3

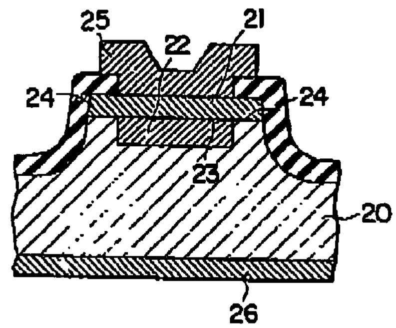



FIG. 4a

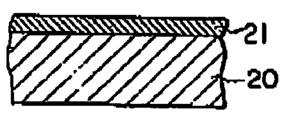



FIG. 4b

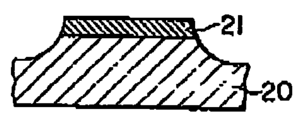



FIG. 4c

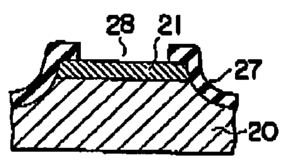
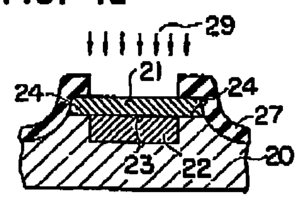



FIG. 4d



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Sheet 2

FIG. 4e

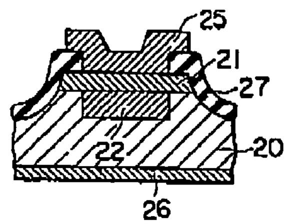



FIG. 5a

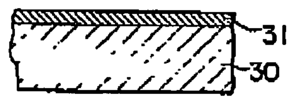



FIG. 5b

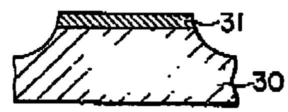



FIG. 5c

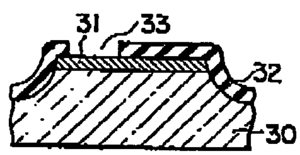



FIG. 5d

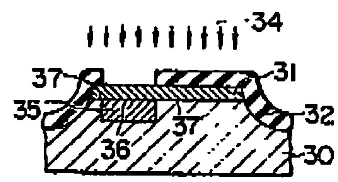



FIG. 5e

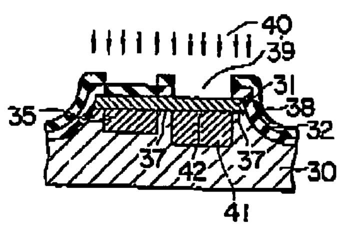
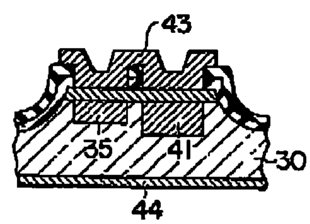



FIG. 5f



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Sheet 3

FIG. 6